## Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

**Listing of claims:**

1. (**Currently Amended**) A method of forming gates in a semiconductor device having a non-linear top profile, the method comprising the steps of:

forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device;

depositing a dummy gate polysilicon layer ~~and a hard mask layer~~ on the dummy gate insulating layer ~~sequentially~~;

**depositing a hard mask layer on the dummy polysilicon layer;**

patterning the hard mask layer into a mask pattern; ~~and~~

**forming a plurality of dummy gates by** patterning the dummy gate polysilicon layer and the dummy gate insulating layer using the mask pattern as an etch barrier,

**wherein** ~~creating~~ a plurality of **the mask patterns is formed on the dummy gates** ~~patterned dummy gate polysilicon and insulating layers each having sidewalls~~,

wherein **a number of the plurality of** the **dummy gates** ~~patterned dummy gate polysilicon and insulating layers~~ are formed on the semiconductor substrate ~~and~~ **while another number of the plurality of dummy gates are formed** on the field

oxide layer,

**wherein the mask patterns on the dummy gates formed on the field oxide layer is at a higher distance when measured from the surface of the semiconductor substrate than the mask patterns on the dummy gates formed on the semiconductor substrate**;

forming **a** spacer~~s~~ at **each of** the **two** sidewalls of **each of** the ~~**patterned**~~ dummy gate ~~**polysilicon and insulating layers**~~;

depositing an insulating interlayer on the resultant structure after forming the spacers;

**performing a non-linear planarization by performing chemical mechanical polishing (CMP) process to polish away the insulating interlayer formed above the mask patterns and the mask patterns, exposing the patterned dummy gate polysilicon layer of each dummy gate,**

~~**exposing a surface of the patterned dummy gate polysilicon and insulating layers by carrying out an oxide layer chemical mechanical polishing (CMP) process utilizing a first high selection ratio sufficient to polish the insulating interlayer but insufficient to polish the patterned dummy gate polysilicon and insulating layers,**~~

wherein the first high selection ratio between the insulating interlayer and the dummy gate polysilicon layer is over 20;

**wherein the length of each dummy gate formed on the semiconductor substrate and the length of each dummy gate formed**

**on the field oxide are identical, and**

**wherein the surface of the polished dummy gate and the insulating layer is wave-like due to the height difference between the dummy gates formed on the field oxides and those formed on the semiconductor substrate;**

forming a damascene structure by removing the patterned dummy gate polysilicon and insulating layers using the insulating interlayer as another etch barrier; **and**

depositing a gate insulating layer and a gate metal layer on the entire surface of the semiconductor substrate having the damascene structure~~; and~~

~~exposing a surface of the insulating interlayer by carrying out a metal CMP process utilizing a second high selection ratio sufficient to polish the metal layer but insufficient to polish the insulating interlayer, wherein the second high selection ratio between the insulating interlayer and the gate metal layer is over 50, so as to result in a structure wherein the heights of the resulting metal gates on the field oxide layer are at substantially the same height as the resulting metal gates on the active area~~.

2. (Original) The method of claim 1, wherein the dummy gate polysilicon layer is formed to a thickness of from 1300 to 2000Å.

3. (Original) The method of claim 1, wherein the insulating interlayer is formed to a thickness of from 4000 to 5000Å.

4. (Cancelled)

5. (Previously Presented) The method of claim 1, wherein the insulating interlayer chemical mechanical polishing uses a slurry including $CeO_2$ particles.

6. (Previously Presented) The method of claim 5, wherein the pH of the slurry, including $CeO_2$ particles, is set between 3 and 11.

7. (Cancelled)

8. (Previously Presented) The method of claim 1, wherein the metal chemical mechanical polishing uses slurry for a metal layer.

9. (Previously Presented) The method of claim 8, wherein the pH of the slurry for a metal layer is set between 2 and 7.